

PACKET MANAGER INTERRUPT MAPPER

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ABSTRACT OF THE DISCLOSURE

[0101] A multiprocessor switching device substantially implemented on a single CMOS integrated circuit is described in connection with an interrupt mapper for informing a plurality of processors about system-related functions for a plurality of channels. Using status registers containing interrupt status information for the plurality of channels, interrupt sources are specifically assigned to individual processors in the multiprocessor device so that the assigned processor can efficiently determine the source and priority of an interrupt by reading the register information.